REMARKS

In response to the above-identified Office Action, Applicant respectfully requests reconsideration in view of the following remarks. In this response, Applicant has not added, amended, or cancelled any claims. Accordingly, claims 1-31 remain pending in the application.

I. Objections to the Specification

The Examiner has objected to the lack of a "Cross-Reference to Related Applications" paragraph. The Applicant is unaware of a requirement to include such a paragraph where priority from another application is not requested. Applicant notes that Application No. 09/837,034 (the '034 Application) was filed June 2, 2001 by Applicant. The '034 Application may share some material with the present application. Applicant respectfully requests the Examiner provide a citation to the appropriate source of authority supporting the Examiner's objection. Applicant believes reference to other applications is optional where no priority is claimed and notice is given. Accordingly, reconsideration and withdrawal of this objection is requested.

The Examiner has also objected to the specification for containing "significant amount of prior art contents." Applicant is unaware of any specific sections of the specification in the "Detailed Description of the Invention" that are exclusively related to prior art and not discussed in the context of the present invention. Thus, the Applicant invites the Examiner to identify any such section of the detailed description of the invention. Further, Applicant is unaware of any requirement to make such an amendment and requests the Examiner cite the relevant source of authority for such a requirement. Accordingly, reconsideration and withdrawal of this objection to the specification are requested.

The Examiner has also objected to the title of the invention by requiring a title that is "clearly indicative of the invention to which the claims are directed." However, the suggested title of the invention proposed by the Examiner is inaccurate and not indicative of the claimed invention. The claimed invention is not related to a dedicated exception handling processor. Rather, the current title accurately describes the claimed invention as related to handling exceptions in a multi-

processing environment. In fact, this is reflected in the preamble of independent claim 1. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the objection to the title.

II. Objections to the Drawings

The Examiner has objected to Figure 1 "because only that which is old is illustrated." The Examiner has required amendment to claim 1 to indicate that the drawings relate to prior art by including the legend "prior art." Applicant respectfully disagrees with this objection. Figure 1 includes a processor 102 and processor 104 which embody the claimed invention and which Applicant believes is not taught by prior art. Processor 102 and processor 104 implement the claimed methods and contain the claimed apparatus or a part of the claimed apparatus. Thus, Figure 1 includes elements which are not old and thus Figure 1 would not properly be identified as prior art. Accordingly, reconsideration and withdrawal of the objection to Figure 1 are requested.

III. Claims Rejected Under 35 U.S.C. §103

Claims 1-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,651,163 issued to Kranich, et al. (hereinafter "Kranich") in view of U.S. Patent No. 6,425,039 issued to Yoshioka (herinafter "Yoshioka"). Applicant respectfully disagrees for the following reasons.

In order to establish a *prima facie* case of obviousness, the Examine must show that each element of a claim is taught or suggested by the combined prior art. In regard to claims 1, 12 and 21, each of these claims include the elements of determining an identification of a processor based on a query that is internal to that processor. For example, claim 1 includes the elements "a processor to determine an identification of the processor based on a query that is internal to the processor." See claim 1, lines 7 and 8. On page 4 of the Office Action, the Examiner indicates that Figure 12 teaches these elements of claims 1, 12 and 21. Specifically, the Examiner asserts control device 300 and mapping table unit 350 illustrated in Figure 12 teach these elements of claims 1, 12 and 21. However, control device 300 and constituent mapping table unit 350 are not internal to any processor. See Figure 2 and col. 9, lines 32-38 and col. 10, lines 37-40 of Kranich. Kranich

clearly describes thread control device 300 as external to the processors in a multiprocessor system taught by Kranich. Thus, thread control device 300 and its internal component mapping table unit 350 (See Figure 3a) are not internal to a processor. The Examiner states on page 4 of the Office Action that the mapping table unit "may have a number of entries equal to the number of processors in a multiprocessor computer" that are "indexed with a logical processor number 1302." Thus, Kranich does not teach or suggest a query internal to a processor to determine identification of the processor. Rather, Kranich teaches a system where thread control device 300 may contain a mapping table 350 that is external to the processors in a multiprocessing system. Therefore, the Examiner has failed to establish that Kranich teaches or suggests a processor to determine an identification of the processor based on a query that is *internal* to that processor as claimed in claims 1, 12 and 21.

Further, Yoshioka does not cure these defects of Kranich. The Examiner has not indicated and Applicant has been unable to discern any part of Yoshioka that teaches or suggests a processor to determine an identification of the processor based on a query that is internal to the processor. Thus, the Examiner has failed to establish that Kranich in view of Yoshioka teaches or suggests each of the elements of claims 1, 12 and 21. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 1, 12, and 21 are requested.

In regard to claims 2-6, 13-16, and 22-26, these claims depend from independent claims 1, 12, and 21 and incorporate the limitations thereof. Thus, at least for the reasons mentioned in regard to claims 1, 12 and 21, these claims are not obvious over Kranich in view of Yoshioka. Accordingly, recommendation and withdrawal of the obviousness rejection of these claims are requested.

In regard to claims 8, 17, and 28, these claims include the elements of a processor that reads a bit within an internal register to determine the identification of the processor in a multiprocessor system. For example, claim 8 includes the elements of a "processor to read a bit within an internal register to determine an identification of the processor in the multiprocessor system." See claim 8, lines 10 and 12. The Examiner cites col. 4, lines 64 - col. 7, line 38 of Kranich as teaching these

elements of claims 8, 17, and 28. Further, the Examiner discusses on page 9 of the Office Action that this section of Kranich describes a processor that supports out of order execution and employs a reorder buffer to track the program sequence of instructions to be executed. It is unclear to Applicant what relevance this has to the claimed elements. Applicant has reviewed the cited section of Kranich and has been unable to discern any part therein that teaches or suggests a processor that reads a bit within an internal registration to determine an identification of a processor of a multiprocessor system.

Yoshioka does not cure these defects of Kranich. The Examiner has not indicated and Applicant has been unable to discern any part of Yoshioka that teaches or suggests these elements of claims 8, 17 and 28. Therefore, Kranich in view of the Yoshioka does not teach or suggest each of the elements of claims 8, 17 and 28. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 8, 17 and 28 are requested.

In regard to claims 9-11, 18-20 and 29-31, these claims depend from claims 8, 17 and 28 respectively, and incorporate the limitations thereof. Thus, at least for the reasons mentioned in regard to claims 8, 17 and 28, these claims are not obvious over Kranich in view of Yoshioka. Further, the Examiner has not indicated any part of Kranich or Yoshioka that teaches the elements of each of these claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

Claims 1, 8, 12, 17, 21 and 28 stand rejected under 35 U.S.C. § 103 as unpatentable over U.S. Patent Application No. 2002/007131 by Brenner, Jr., et al. (hereinafter "Brenner") in view of U.S. Patent No. 6,006,247 issued to Browning, et al. (hereinafter "Browning"). Applicant notes that the Examiner in the Office Action after stating the initial grounds for rejection over Brenner in view of Browning consistently cites Yoshioka instead of Browning which appears to be a clerical error. The cited sections of Yoshioka are unrelated to the arguments of the Examiner and the claims of the application. Thus, the Applicant has discerned that the Examiner has intended to cite Browning and that the citation Yoshioka in this section of the office action is a clerical error.

In regard to claims 1, 12 and 21, these claims include the elements of a number of

instructions that cause a processor to determine an identification of the processor based on a query that is internal to the processor. For example, claim 1 includes the elements of a "number of instructions cause the processor to determine an identification of the processor based on a query that is internal to the processor." See claim 1, lines 7 and 8. The Examiner admits that Brenner does not teach these elements of claims 1, 12 and 21. The Examiner relies on Browning and cites Figure 2 of Browning where a processor list 44 is illustrated as part of global memory 36. However, global memory 36 which includes the processor list is external to the processors in a multiprocessor system and thus Figure 2 does not support the Examiner's assertion. Processor list 44 of global memory 36 as illustrated in Figure 2 of Browning does not teach a number of instructions that cause a processor to determine an identification of a processor based on a query that is *internal* to the processor. Rather, processor list 44 in global memory 36 of Browning is external to the processors in the multiprocessor system of Browning. See Figure 2 and col. 4, lines 6-45. Further, processor list 44 in global memory 36 does not track an identification of processors in the multiprocessor system, rather it identifies a thread running on each processor in the multiprocessor system. See col. 4, lines 37-40 of Browning. Therefore, Brenner in view of Browning does not teach or suggest each of the elements of claims 1, 12 and 21. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 1, 12 and 21 are requested.

In regard to claim 8, 17, and 28, these claims include the elements of a number of instructions causing a processor to read a bit within an internal register to determine the identification of a processor in a multiprocessor system. See, for example, lines 10-12 of claim 8. As discussed above, in regard to claims 1, 12 and 21, the Examiner admitted in relation to claims 1, 12, and 21 that Brenner does not teach an internal query to determine identification of the processor which would include reading a bit from an internal register as claimed in claims 8, 17 and 28. The Examiner further admits that Brenner does not teach the use of common interrupt handling vector.

Browning does not cure these defects of Brenner. The Examiner again cites Figure 2 and processor list 44 of global memory 36 as teaching the identification of a processor in a

multiprocessor system. For the reasons mentioned above, Browning does not in fact teach these elements of claims 8, 17 and 28. Further, the Examiner has not indicated any part of Browning that teaches common interrupt handling vectors. Therefore, the Examiner has failed to establish that Brenner in view of Browning, teaches or suggests each of the elements of claims 8, 17 and 28. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-31 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 4/5, 2004

Jonathan S. Miller, Reg. No. 48,534

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 5, 2004.

4-5-04

Lillian E. Rodriguez April 5, 2004